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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,948	09/19/2003	Stephen J. Smith	174/161 Cont	7049

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EXAMINER	
SURYAWANSHI, SURESH	
ART UNIT	**PAPER NUMBER**
2115	

DATE MAILED: 03/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/666,948	SMITH ET AL.	
	Examiner	Art Unit	
	Suresh K. Suryawanshi	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/22/05 amendments*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,15-18 and 28-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15-18* is/are allowed.

6)☒ Claim(s) *1-4 and 28* is/are rejected.

7)☒ Claim(s) *29-33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/22/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. ____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-4, 15-18 and 28-33 are presented for examination.

2. The text of those sections of Title 35 U.S. Code not included in this action can be found in the prior office action.

3. The examiner withdraws the rejections on claims 15-18 in view of amendment to claim 15 and applicants' arguments.

4. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sharrit et al (US Patent 5,999,990; hereinafter Sharrit) in view of Vernon et al (EP 0 901 351 A2; hereinafter Vernon).

5. As per claim 1, Sharrit discloses a reconfigurable computer system comprising:

at least one programmable logic resource [col. 1, lines 54-59; a plurality of reconfigurable resource units (RRUs)];

programmable logic coupled to the central processing unit [Fig. 3, 4; col. 2, lines 55-58; col. 5, lines 36-38, 58-60], wherein the programmable logic is reconfigurable to optimize the

ability of the computer system to handle a given application [col. 1, lines 54-61; col. 2, lines 35-45; col. 6, lines 23-35]; and

a secondary storage device that stores configuration data for the programmable logic, wherein the secondary storage device is a mass storage device [col. 5, lines 33-57; a hard disk].

Sharrit does not expressly disclose about at least one programmable logic resource that is at least partially configured as a central processing unit. But a routineer in the art would know that a programmable logic resource could be implemented or programmed to function as a central processing unit. However, Vernon explicitly discloses implementing at least one programmable logic resource as a central processing unit [col. 3, lines 5-10; FPGA is configured to provide the functions of a microprocessor]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both are related to programmable logic circuits and their implementations. Moreover, one can clearly see the benefit of utilizing programmable logic resources as they can be readily reconfigured as needed according to the current system requirements. Further, there is a benefit of having simpler and smaller circuit boards for producing small and convenient user devices.

6. As per claim 2, Sharrit discloses that the system further comprising non-volatile memory coupled to the programmable logic [col. 5, lines 33-56; a hard disk drive].

7. As per claim 3, Sharrit discloses that the system further comprising random-access memory coupled to the programmable logic [col. 5, lines 33-56; RAM].

8. As per claim 4, Sharrit discloses that the system further comprising input-output circuitry [Fig. 1; col. 2, lines 28-31; input/output port].

9. Claim 28 is rejected under 35 U.S.C. 102(e) as being anticipated by Sharrit et al (US Patent 5,999,990; hereinafter Sharrit).

10. As per claim 28, Sharrit teaches a method for managing resources in a computer that contains programmable logic resources that are reconfigurable to optimize the ability of the computer to handle a given application having multiple functions [The communicator includes a controller for dynamically allocating the reconfigurable resource units (col. 1, lines 54-61). The controller includes a resource allocation unit that is operative for allocating the resources of the plurality of RRUs (col. 7, lines 15-33).] comprising :

during run-time [col. 1, lines 54-61; during operation; col. 6, lines 26-29; currently on signal bus], using a virtual computer operating system to autonomously determine whether to use a hardware implementation or a software implementation for a given one of the multiple functions of the given application [The controller, implemented in software, determines whether a signal currently on signal bus will be processed in hardware (in FPGA) or in software

(in DSP). Reconfigurable resource units (RRUs) are dynamically altered during operation. Please see col. 1, lines 54-64; col. 2, lines 35-45; col. 6, lines 23-35, 54-57.].

Allowable Subject Matter

11. Claims 29-33 are objected to as being dependent upon a rejected base claim 28, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. Claims 15-18 allowed.

Response to Arguments

13. Applicant's arguments filed 12/22/05 have been fully considered but they are not persuasive.

14. In the remarks, applicants argued in substance that (1) the hard disk drive does not store configuration data for programmable logic as recited in applicants' independent claim 1; (2) the determination of whether to process data in either hardware or software is pre-defined based on the configuration files used to reconfigure an RRU and is not autonomously determined during run-time as recited in applicants' independent claim 28.

15. As to point (1), Sharrit clearly discloses that a mass storage unit, such as a hard disk drive, is used for storing a library of programs [col. 5, lines 46-49]. These libraries of programs include configuration files that can be used to reconfigure the plurality of RRUs [col. 1, lines 61-64]. Therefore, Sharrit clearly discloses about a mass storage device for storing configuration data for programmable logic as recited in applicants' independent claim 1.

16. As to point (2), Sharrit clearly discloses that a plurality of reconfigurable resource units (RRUs) are dynamically altered during operation for performing any of a variety of processing tasks [col. 1, lines 54-59]. Further, Sharrit discloses that a particular RRU can be set up to perform one set of processing functions at one moment and a different set of processing functions at another moment [col. 2, lines 35-45]. Furthermore, Sharrit adds that RRU is a hybrid unit that allows controller to specify whether a signal currently on signal bus will be processed in hardware (in FPGA) or in software (in DSP) [col. 6, lines 23-35]. Therefore, Sharrit clearly discloses that the determination of whether to process data in either hardware or software is autonomously determined during run-time as recited in applicants' independent claim 28.

Conclusion

17. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K. Suryawanshi whose telephone number is 571-272-3668. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sks
March 1, 2006

THOMAS LEE
SUPERVISORY PATENT EXAMINER
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